Notice of Allowability	Application No.	Applicant(s)	
	10/766,648	MCCAFFREY ET AL.	
	Examiner	Art Unit	
	Asif Khokhar	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *paper filed on 08/17/2007*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Drawings

1. Drawings are accepted by the examiner.

Allowable Subject Matter

2. The restriction requirement, as set forth in the Office action mailed on 07/18/2007, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). **The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.** Claim 6-10,12-16,21-25, directed to second embodiment no longer withdrawn from consideration because the claim(s) requires all the limitations of an allowable claim.

3. Claims 1-25 are allowable.

4. The prior art of the record does not suggest or discloses:

With regard to claim 1, a method of addressing imagers providing a first multiplexer having a vertical select input and n outputs, wherein each of said n outputs is connected to one of said Vmode terminals of said imagers; providing a second multiplexer having a horizontal select input and n.times.m outputs wherein each said output is connected to said select terminal of one of said imagers; applying a vertical input signal to said vertical select input of said first multiplexer thereby producing said first selecting signal at one of said Vmode output lines; and applying a horizontal input signal to said horizontal select input of said second multiplexer

thereby sequentially producing said second selecting signal at said select terminal of one of said imagers.

With regard to claim 2, a method of accessing an imager array which comprises accessing one line of one said imager corresponding to said line address, said column counter, and said row counter; thereafter testing said column counter for equality to m-1 wherein, if not equal, said column counter is incremented and said step of accessing one line is repeated and wherein, if equal, said column counter is reset; thereafter testing said line address for equality to total lines in each said imager wherein, if not equal, said line address is incremented and said step of accessing one line is repeated, and wherein, if equal, said line address is reset; and thereafter testing said row counter for equality to n-1 wherein, if not equal, said row counter is incremented and said step of accessing one line is repeated, and wherein, if equal, said step of accessing all is completed.

With regard to claim 8, accessing one line of one said imager corresponding to said line address, said column counter, and said row counter; thereafter testing said column counter for equality to m-1 wherein, if not equal, said column counter is incremented and said step of accessing one line is repeated and wherein, if equal, said column counter is reset; thereafter testing said line address for equality to total lines in each said imager wherein, if not equal, said line address is incremented and said step of accessing one line is repeated, and wherein, if equal, said line address is reset; and thereafter testing said row counter for equality to n-1 wherein, if not equal, said row counter is incremented and said step of accessing one line is repeated, and wherein, if equal, said step of accessing all is completed.

With regard to claim 11, a first multiplexer having an input and a plurality of outputs wherein said input is connected to a column counter and wherein each said output is connected to said output enable input of one of said imagers; and a second multiplexer having an input and a plurality of outputs wherein said input is connected to a row counter and wherein each said output is connected to said Vmode input of each said imager in one of said rows.

With regard to claim 21, a first multiplexer having an input and a plurality of outputs wherein said input is connected to a sum of a column counter and a row counter and wherein each said output is connected to said output enable input of one of said imagers; a second multiplexer having an input and a plurality of outputs wherein said input is connected to a row counter and wherein each said output is connected to said Vmode input of each said imager in one of said rows a first divider having an input and an output wherein said input is connected to a horizontal clock signal and wherein said output is said column counter; and a second divider having an input and an output wherein said input is connected to said line address and wherein said output is said row counter.

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sauer US 5134488 discloses an X-Y addressable imager, which is controlled by electrically controlling the effective photonic charging time of each pixel in each frame time of operation. But Sauer '488 does not discloses that column counter is generated by dividing horizontal clock by the number of bits in each line and row counter is generated by dividing line address by total lines in each imager.

Nakamura et al US6507365 discloses an imaging area where unit cells with photodiodes acting as pixels are arranged two-dimensionally, read lines for driving the read transistors in each pixel row, vertical selection lines for driving the vertical selection transistors in each pixel row, a vertical driving circuit for selectively driving vertical selection lines, vertical signal lines for outputting the signal from each unit cell in the pixel rows driven sequentially, and a row selection circuit for controlling the vertical driving circuit in such a manner that the vertical driving circuit drives the read transistors in each pixel row with the desired signal storage timing. But Nakamura '365 does not discloses two terminal (select terminal and Vmode terminal) and two multiplexers having horizontal and vertical input.

Sauer et al US5973311 discloses Pixel array including a high-resolution mode and a low-resolution mode and method of reading out the pixel array in a high and low-resolution mode. The pixel array includes a first signal line and a second signal line. An array of pixel elements are provided, each pixel element coupled to the first signal line or the second signal line. A switch mechanism is provided for coupling the first signal line to the second signal line. But Sauer '311 does not disclose two multiplexers having horizontal and vertical input.

Matsunaga et al US6091449 discloses In an MOS-type solid-state imaging apparatus, plural unit cells are arranged in a two-dimensional matrix, unit cells in one horizontal line (row) are selected by a vertical address circuit, and vertical signal lines to which outputs from the unit cells in one vertical line (column) are supplied are selected by a horizontal address circuit, thereby sequentially outputting signals from the respective unit cells. Each unit cell includes an output circuit for outputting an output from a photodiode to a vertical signal line, photodiodes connected in parallel to the output circuit, and a selection switch for selecting one of the

photodiodes and connecting it to the output circuit. But Matsunaga '449 does not disclose a horizontal clock dividing by number of bits in each said line and two multiplexers having horizontal and vertical input.

Yoneyama et al US5719626 discloses A solid-state image pickup device includes a plurality of pixels each having a light-receiving element and an amplification element, and a scanning circuit having a shift register constituted by connecting a plurality of circuit stages in tandem and capable of almost simultaneously setting outputs from the plurality of circuit stages in a predetermined logical state upon reception of a predetermined control signal. But Yoneyama '626 does not disclose a horizontal clock dividing by number of bits in each said line and two multiplexers having horizontal and vertical input.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asif Khokhar whose telephone number is (571) 270-3221. The examiner can normally be reached on Monday- Friday 7:30am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Ho can be reached on 571 272 7365. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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TUAN HO
PRIMARY EXAMINER